

Docket No. TD-155

## REMARKS

Examiner Tung is thanked for the recent Office action. No claims are amended at this time. All outstanding rejections are hereby traversed. Favorable reconsideration, based on the following comments, is respectfully requested.

### Review of the References

Meinerth appears to describe a unified memory system where the CPU and graphics processor (GP) access the same memory. This memory is divided into a main memory and a frame buffer, but is still unified. Because of Meinerth's configuration, however the CPU addresses memory, the GP must do likewise and take care not to access stale or invalid data. The CPU uses a virtual memory and caches so the GP of Meinerth needs to do the same (unless the accessible memory is locked down, contiguous, and non-cached). Meinerth does not appear to teach or suggest page faulting of texture data, and does not teach dedicated graphics memory. Specifically, part of the advantage of Meinerth is that both the GP and CPU access the same memory.

Blinn appears to discuss, in general terms, the concept of page faulting in a computer system with a graphics processor. It does not appear to teach or in any way address managing page faulting of texture data without CPU intervention.

### Art Rejections

Examiner has rejected all pending claims (*i.e.*, claims 1-5, 7-10, and 12-22) under 35 USC 103(a) as unpatentable over Meinerth et al. (USPN 6124865) in view of Jim Blinn ("The Truth About Texture Mapping"), hereinafter referred to as "Meinerth" and "Blinn", respectively.

In rejecting claim 1, Examiner states in part,

Meinerth teaches a computer system...comprising a graphics accelerator unit...which can transfer data (not particularly suggest that the data is

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**texture data** for the graphics processing unit and the transfer of data is when/after the **page fault** is occurred) from main memory (140) to frame buffer (164)....

[Emphasis in original.]

Hence, Examiner agrees that Meinerth does not teach page faulting, nor does it teach page faulting of texture data. Examiner seeks to cure this lack of teaching in Meinerth by citing Blinn, about which Examiner states:

Blinn teaches page fault occurs when accessing texture data from main memory fails and the data is transfer from another storage device into the memory.... It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teaching of Blinn into the system of Meinerth in order to add realism to the computer generated graphic in the 3D space. Therefore at least claim 1 would have been obvious.

Hence, Examiner has cited Blinn for the general teaching that when a page fault of texture data occurs, the texture data is moved from one storage to another.

**A. Frame buffer (164) of Meinerth cannot hold texture data, and therefore cannot properly be used to fulfill the claimed limitation of, "page faulting of texture data..." as claimed.**

Applicant respectfully submits that the cited references, even if they may be properly combined (which Applicant does not stipulate), fail to teach or suggest the claimed limitations of at least claim 1. Claim 1 states:

1. A computer system, comprising:  
a graphics accelerator unit which manages page faulting of texture data invisibly to the host processor.

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A frame buffer is computer memory allocated to hold graphics information for a single frame to be displayed on a screen, and comprises color values for each pixel of the screen. A frame buffer is not used to store texture data, and Meinertsh does not teach or suggest that the frame buffer would store texture data. Examiner admits this, and seeks to cure this deficiency by citing Blinn. However, Blinn only teaches known page faulting of texture data, which invokes the CPU (*e.g.*, Blinn states, "On big computers and workstations this is all done with a combination of special CPU hardware and operating system code...."), and which presumably includes memory other than the frame buffer to store the texture data. The cited combination of references therefore does not fulfill the claimed limitation of, "a graphics accelerator unit which manages page faulting of texture data invisibly to the host processor."

**B. The cited references cannot be properly combined as suggested by Examiner.**

Further, Applicant respectfully submits that the references Meinertsh and Blinn cannot be properly combined as Examiner suggests. Blinn is cited for its teaching that texture data can be transferred on a page fault, but Blinn explicitly refers to the CPU in transferring this data. Meinertsh, on the other hand, allows for normal data transfers (and Examiner admits that these transfers are not page faults of texture data, and in fact the memory to which Examiner suggests the texture data would be stored is actually a frame buffer, which is not used to store texture data), without CPU intervention in some cases. To combine these references, either or both references would have to be significantly modified, as they are inconsistent with one another, and mutually exclusive. No such modifications are taught or suggested in either reference.

Therefore, Applicant respectfully submits that the modifications necessary to properly combine the cited references could only be obtained by referring to the present application, which is an impermissible use of hindsight. "It is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such

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reference fairly suggests to one of ordinary skill in the art." *In re Hedges*, 228 U.S.P.Q. 685, 687 (Fed. Cir. 1986).

There is also no motivation taught or suggested in either reference to make the combination proposed by Examiner. Examiner states that, "It would have been obvious to one of ordinary skill in the art...to combine the teaching of Blinn into the system of Meinerth in order to add realism to the computer generated graphic in the 3D space." However, Meinerth already contemplates graphics processing, as it explicitly includes graphics processor 210, yet does not mention the combination proposed by Examiner. Applicant respectfully submits that this is because Meinerth is inconsistent with Blinn, as mentioned above.

Therefore, because significant modification of the references would be necessary in order to combine the two references, Applicant respectfully submits that it would not have been obvious to one of ordinary skill in the art to make the proposed combination. Therefore, it is respectfully submitted that at least claim 1 is distinguished from the cited references. Favorable reconsideration is respectfully requested.

**C. Meinerth does not teach or suggest a dedicated graphics memory which can store texture data.**

Further, Applicant respectfully submits that claim 2 includes limitations relevant to the argument made above. Claim 2 states:

2. A computer system, comprising:  
a graphics accelerator unit which manages page faulting of texture data, from main memory used by at least one host processor into a dedicated graphics memory, invisibly to the host processor, except when said graphics accelerator unit calls for data which has not recently been present in said memory.

[Emphasis added.]

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Examiner cites Meinerth's frame buffer 164 as the memory in which the texture data is stored. However, as argued above, frame buffer 164 cannot fulfill the claimed limitation of, "page faulting of texture data...into a dedicated graphics memory," in claim 2. The frame buffer, as it is normally understood in the art, is used to store pixel color information for immediate display, and is not used to store texture data.

For this reason and for those argued above with respect to claim 1, it is respectfully submitted that claim 2 is distinguished from the cited reference. Favorable reconsideration is respectfully requested.

With respect to claim 3, Applicant respectfully submits that Examiner has again selectively chosen from the teachings of the cited references (particularly Blinn) without providing teaching or suggestions or motivation in the art to create such a combination.

For example, in rejecting claim 3, Examiner has cited a "second memory management unit" from Meinerth but attributed to that unit an action that is performed in Blinn. Examiner states, on page 3 of the Office action:

Meinerth further teaches...a second memory management unit (FIG. 3, 154...) which manages texture data for said accelerator logic and performs page faulting (Blinn, page 79, col. 1) of said texture data...

Applicant respectfully submits that this combination is improper. Moreover, the examiner may not use the claimed invention as an "instruction manual" or "template" to piece together the teachings of the prior art so that the invention is rendered obvious. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). Such reliance is an impermissible use of hindsight with the benefit of applicant's disclosure. *Id.* A prima facie case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching, suggestion, or incentive supporting the combination. *In re Geiger*, 815 F.2d 686, 688, 2 U.S.P.Q.2d 1276, 1278 (Fed.

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Cir. 1987). In determining obviousness, an applicant's teachings may not be read into the prior art. *Panduit Corp. v. Denison Mfg. Co.*, 810 F.2d 1561, 1575 n. 29, 1 U.S.P.Q. 1593, 1602 n. 29 (Fed. Cir. 1987) (citing need to "guard against hindsight and the temptation to read the inventor's teachings into the prior art"). A determination of the desirability of combining prior art references must be made without the benefit of hindsight afforded by an applicant's disclosure. *In re Paulsen*, 30 F.3d 1475, 1482, 31 U.S.P.Q. 1671, 1676 (Fed. Cir. 1994). A proper *prima facie* case of obviousness cannot be established by combining the teachings of the prior art absent some teaching, incentive, or suggestion supporting the combination. *In re Napier*, 55 F.3d 610, 613, 34 U.S.P.Q.2d 1782, 1784 (Fed. Cir. 1995); *In re Bond*, 910 F.2d 831, 834, 15 U.S.P.Q.2d 1566, 1568 (Fed. Cir. 1990).

For these reasons, it is respectfully submitted that the proposed combination of references is improper for all claims, and, for example, with respect to claim 3.

With respect to claim 4, Examiner again equates the frame buffer 164 of Meinerth with the "local memory" associated with a graphics processor. For the reasons stated above, claim 4 is believed to be distinguished from the cited references.

In rejecting claim 7, Examiner cites the rejection of claim 3. Therefore, for the reasons argued above, claim 7 is believed distinguished from the cited reference.

Claims 14 and 15 are rejected in reference to the argument made against claim 3 by Examiner. Therefore, for the reasons cited above, claims 14 and 15 are believed distinguished from the cited reference.

Claim 17 is rejected in reference to claim 4, and is therefore believed allowable based on the arguments made above.

Claim 20 is rejected with reference to claim 7, and is therefore believed distinguished based on arguments made above.

Claim 22 is rejected with reference to claim 3, and is therefore believed distinguished based on arguments made above.

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Therefore, all independent claims are believed distinguished from the cited references. Because of their dependence on allowable claims, all dependent claims are therefore believed allowable as well.

Favorable reconsideration of all claims is therefore respectfully requested.

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Conclusion

Thus, all grounds of rejection and/or objection are traversed or accommodated, and favorable reconsideration and allowance are respectfully requested. The Examiner is requested to telephone the undersigned attorney or Robert Groover for an interview to resolve any remaining issues.

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Respectfully submitted,



Patrick C. R. Holmes, Reg. No. 46,380  
Attorney for Applicant

**Customer Number 29106**

Groover & Holmes

PO Box 802889

Dallas TX 75380

Tel: 972-980-5840

Fax: 972-580-5841